Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **I OUT1**
2. **I OUT2**
3. **GND**
4. **DB7**
5. **DB6**
6. **DB5**
7. **DB4**
8. **DB3**
9. **DB2**
10. **DB1**
11. **DB0**
12. **N. CS**
13. **N. WR**
14. **VDD**
15. **VREF**
16. **RFB**

**.076”**

**7 8 9 10**

**3 2 1 16 15 14**

**13**

**12**

**11**

**4**

**5**

**6**

**.070”**

**NOTE: PMI recommends that the chip back is isolated from any supply,**

**But if necessary CMOS chips like this may be connected to the positive supply VDD.**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .070” X .076” DATE: 9/23/21**

**MFG: ANALOG DEVICES THICKNESS .020” P/N: AD7524**

**DG 10.1.2**

#### Rev B, 7/19/02